DOCUMENT DESIGNED

FIG. 1A

ASYNCHRONOUS SUBACTION

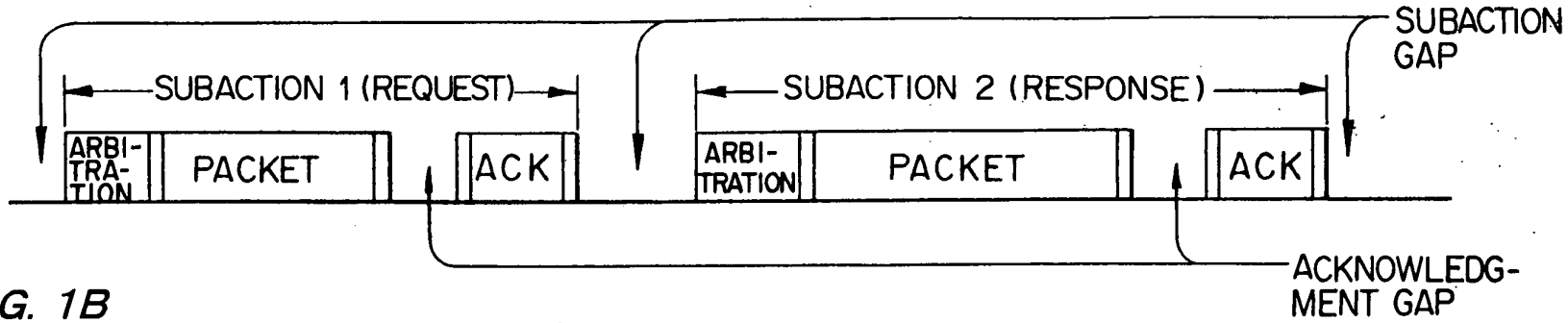
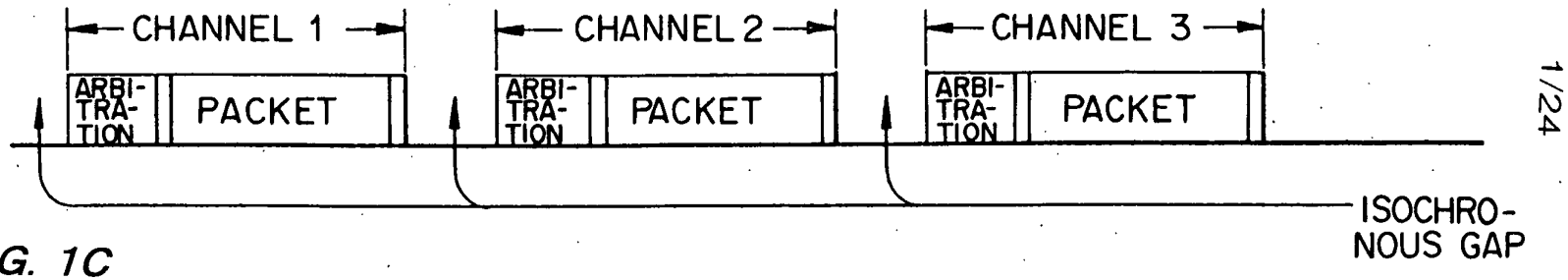


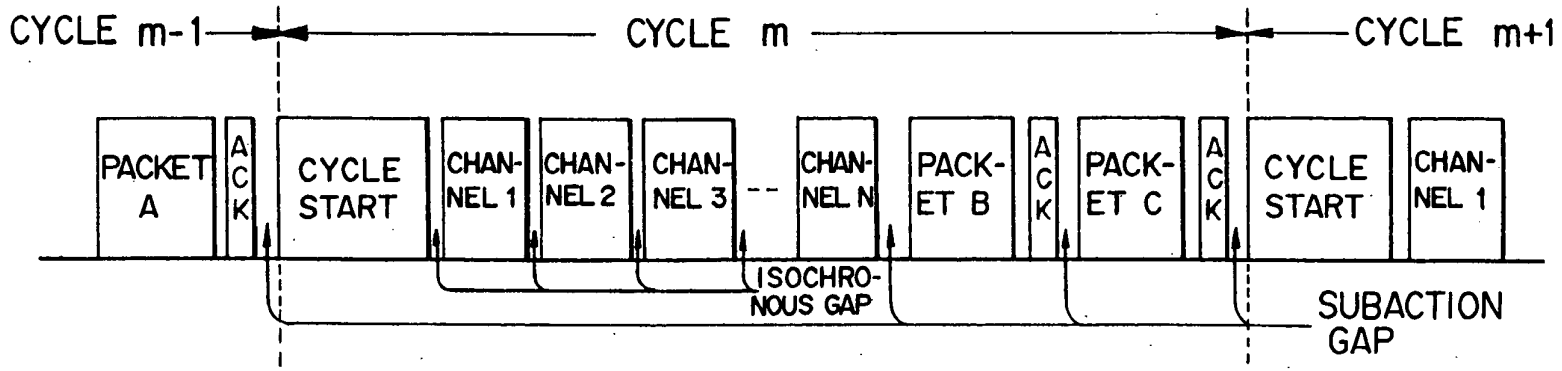
FIG. 1B

ISOCHRONOUS SUBACTION



1/24

FIG. 1C



09/582290

FIG. 2A

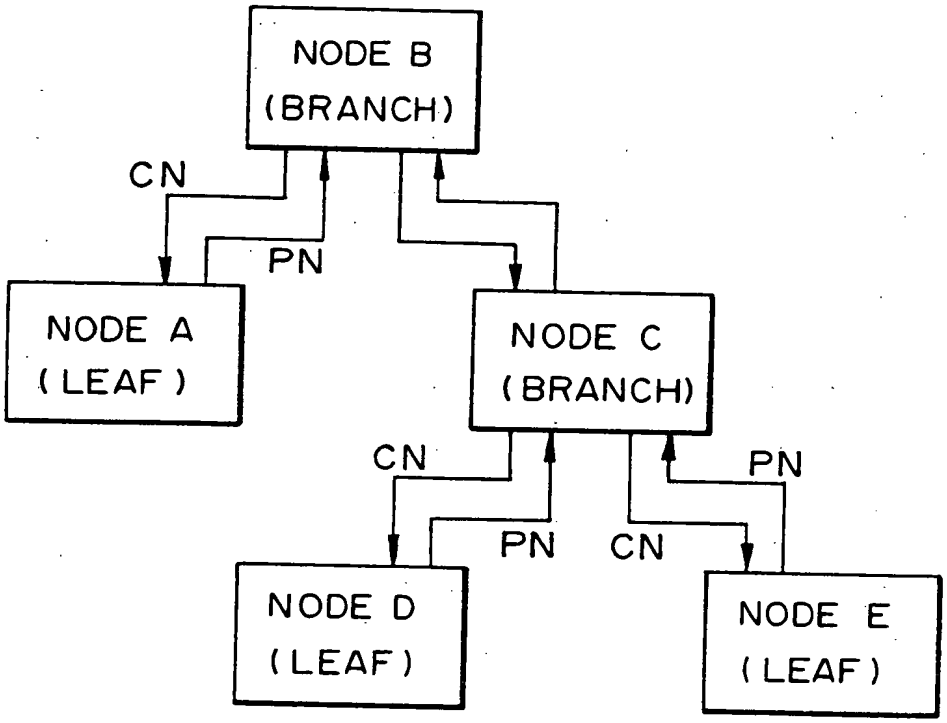

NODE B
(BRANCH)
CN
PN
NODE A
(LEAF)
NODE C
(BRANCH)
CN
PN
PN
CN
NODE D
(LEAF)
NODE E
(LEAF)

FIG. 2B

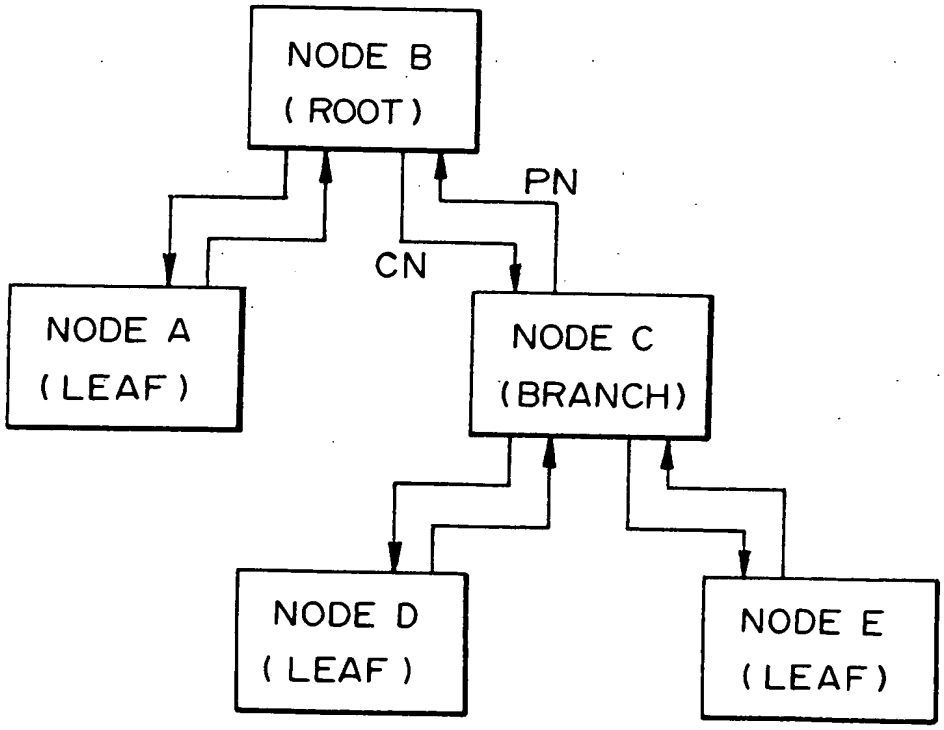

NODE B
(ROOT)
PN
CN
NODE A
(LEAF)
NODE C
(BRANCH)
NODE D
(LEAF)
NODE E
(LEAF)

FIG. 3

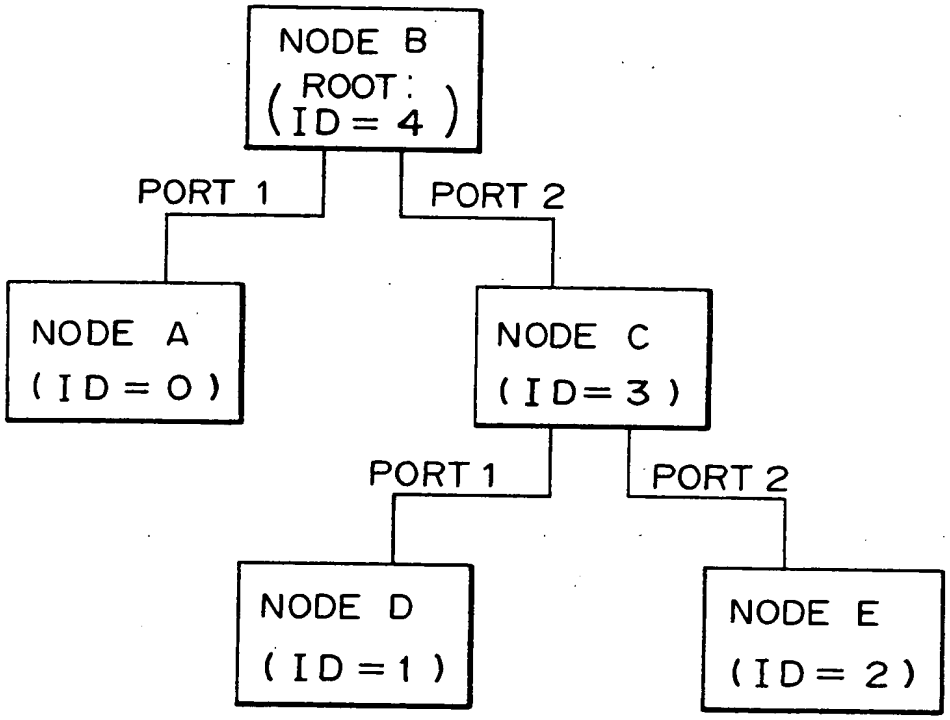

NODE B
ROOT:
(ID = 4)
PORT 1
PORT 2
NODE A
(ID = 0)
NODE C
(ID = 3)
PORT 1
PORT 2
NODE D
(ID = 1)
NODE E
(ID = 2)

FIG. 4A

SELF-ID PACKET #0

	b.31													b.0
0	10	PHY_ID	0	L	gap_cnt	sp	del	C	pwr	p0	p1	p2	i	m
1	INVERSION OF FIRST 32 BITS													

FIG. 4B

SELF-ID PACKETS #1, #2, #3

	b.31													b.0
0	10	PHY_ID	1	n	rsv	pa	pb	pc	pd	pe	pf	pg	ph	r	m
1	INVERSION OF FIRST 32 BITS													

FIG. 4C

LINK-ON PACKET

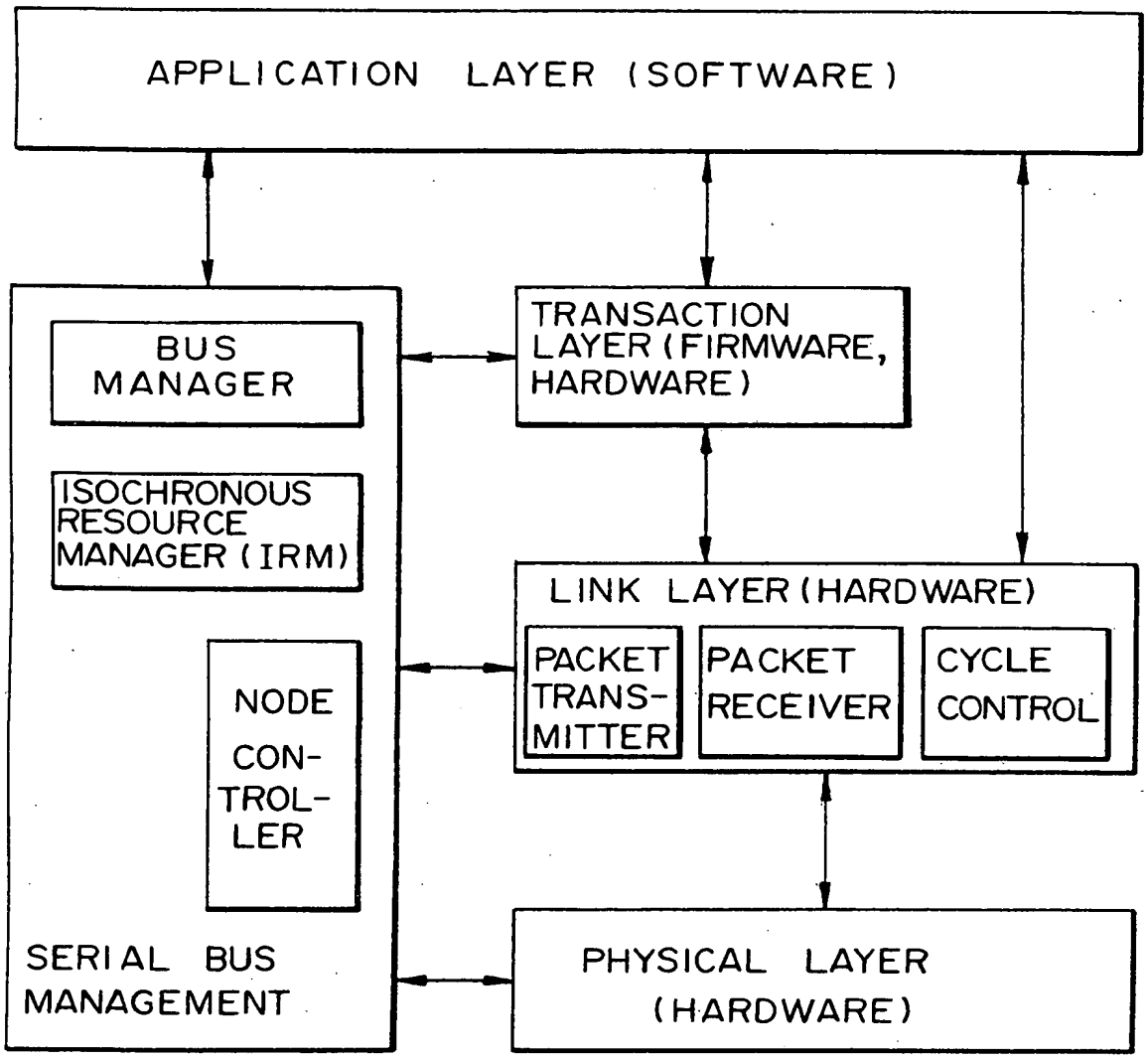
	b.31								b.0
0	01	PHY_ID	0000	0000	0000	0000	0000	0000	
1	INVERSION OF FIRST 32 BITS								

FIG. 4D

PHY CONFIGURATION PACKET

	b.31								b.0
0	00	PHY_ID	R	T	gap_cnt	0000	0000	0000	0000
1	INVERSION OF FIRST 32 BITS								

FIG. 5


APPLICATION LAYER (SOFTWARE)
BUS MANAGER
ISOCHRONOUS RESOURCE MANAGER (IRM)
NODE CON-TROL-LER
SERIAL BUS MANAGEMENT
TRANSACTION LAYER (FIRMWARE, HARDWARE)
LINK LAYER (HARDWARE)
PACKET TRANS-MITTER
PACKET RECEIVER
CYCLE CONTROL
PHYSICAL LAYER (HARDWARE)

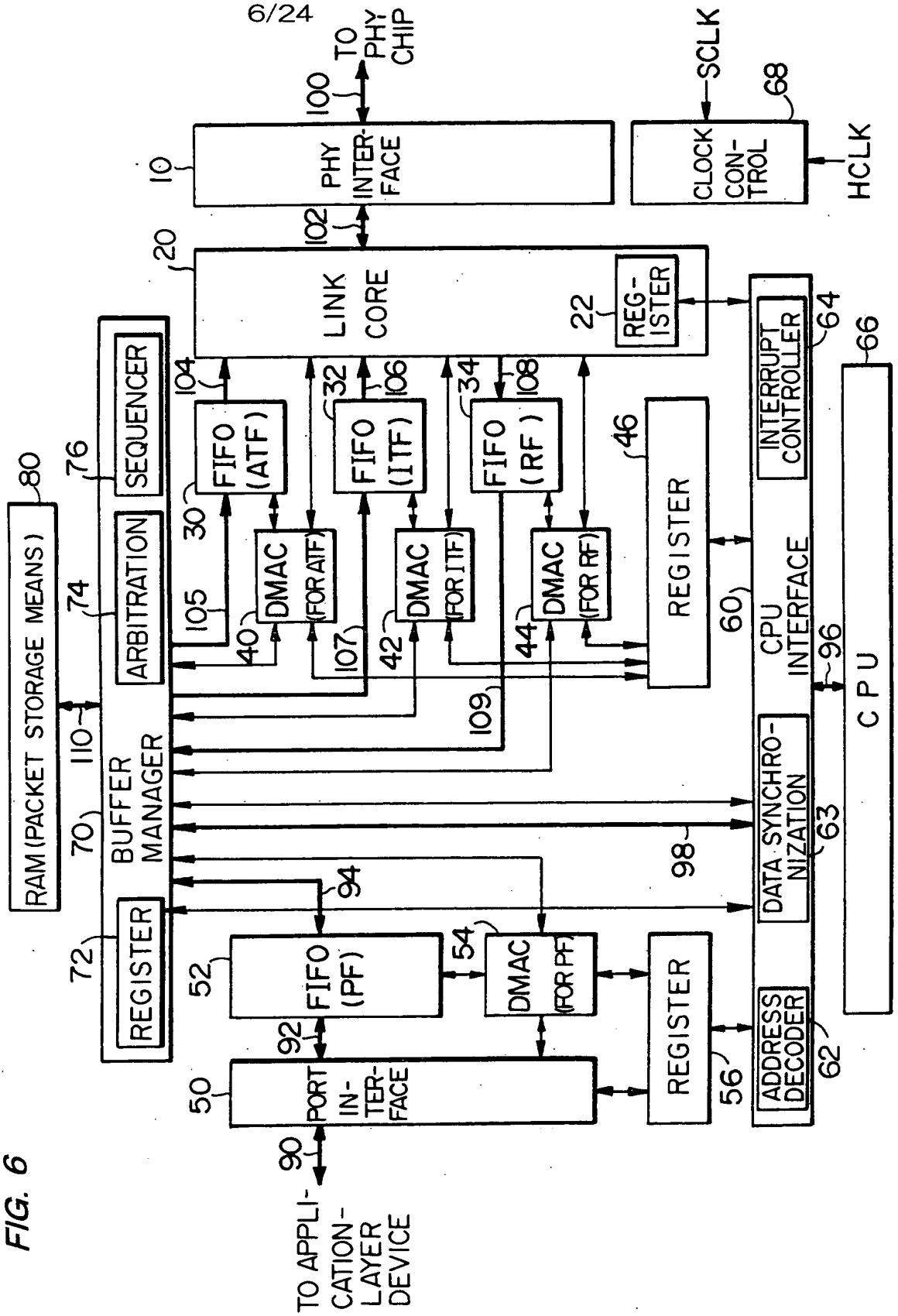
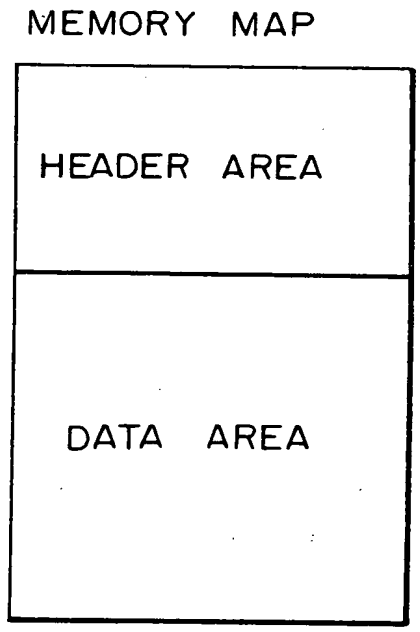

TO PHY CHIP
100
PHY INTER-FACE
10
SCLK
CLOCK CON-TROL
68
HCLK
102
LINK CORE
20
REG-ISTER
22
104
FIFO (ATF)
30
32
106
FIFO (ITF)
34
108
FIFO (RF)
46
INTERRUPT CONTROLLER
64
66
SEQUENCER
76
80
RAM (PACKET STORAGE MEANS)
ARBITRATION
74
105
DMAC (FOR ATF)
40
107
DMAC (FOR ITF)
42
DMAC (FOR RF)
44
REGISTER
60
CPU INTERFACE
96
CPU
109
110
BUFFER MANAGER
70
98
DATA SYNCHRO-NIZATION
63
72
REGISTER
94
52
FIFO (PF)
54
DMAC (FOR PF)
92
50
PORT IN-TER-FACE
90
REGISTER
56
ADDRESS DECODER
62
TO APPLI-CATION-LAYER DEVICE

FIG. 6

FIG. 7



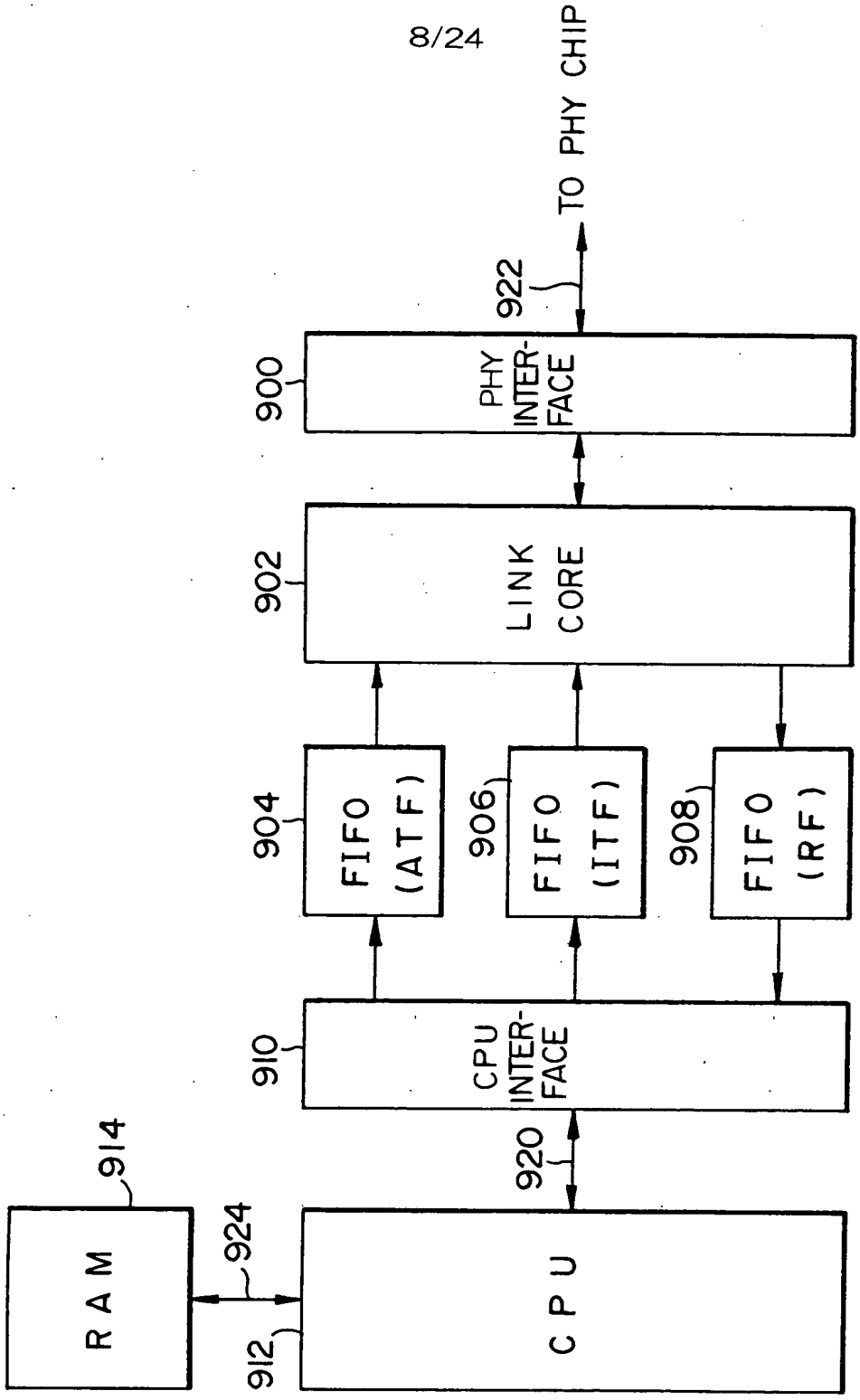

TO PHY CHIP
922
900
PHY INTER-FACE
902
LINK CORE
904
FIFO (ATF)
906
FIFO (ITF)
908
FIFO (RF)
910
CPU INTER-FACE
920
914
RAM
924
912
CPU

FIG. 8

FIG. 9

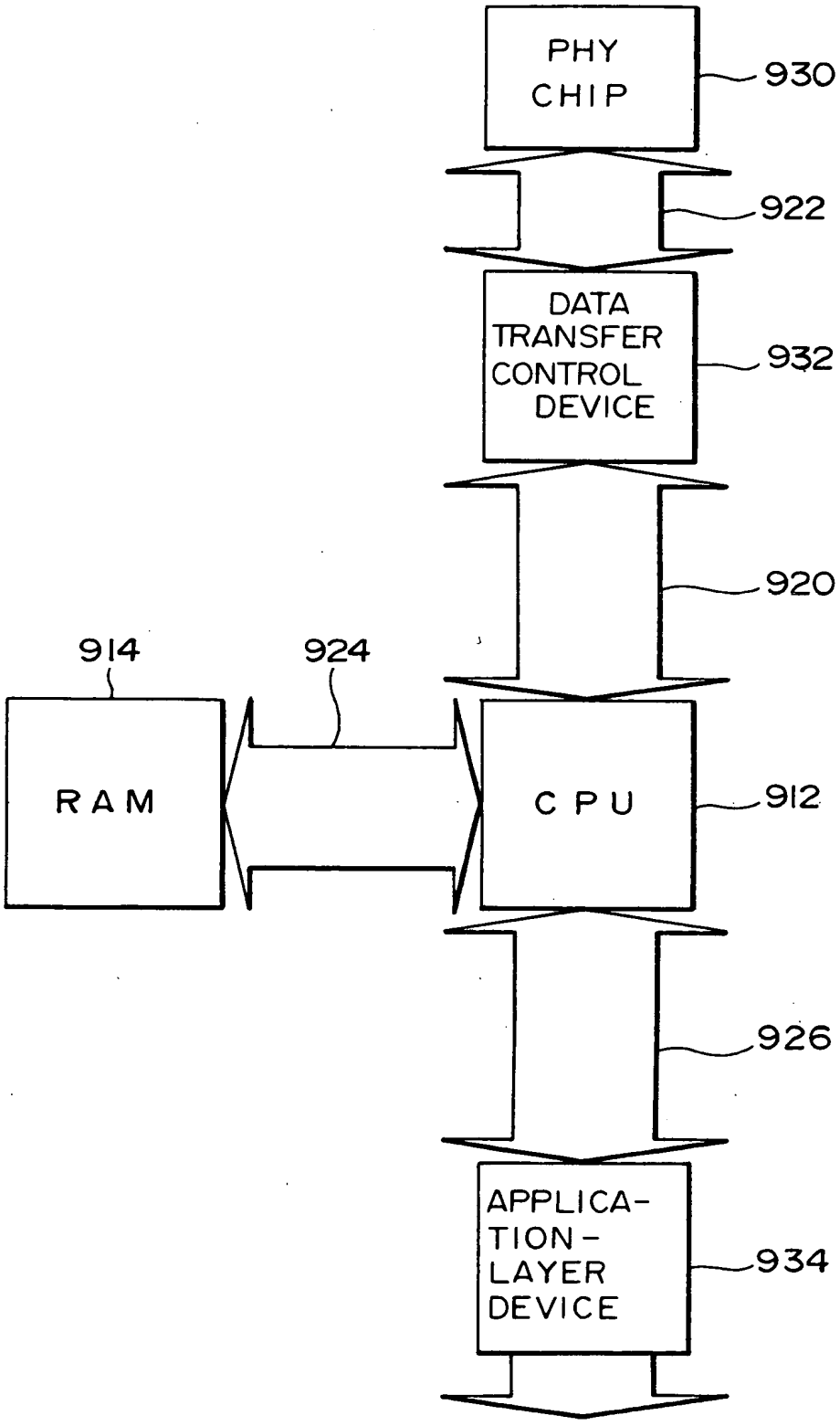

PHY CHIP
930
922
DATA TRANSFER CONTROL DEVICE
932
920
914
924
RAM
CPU
912
926
APPLICA-TION-LAYER DEVICE
934

FIG. 10

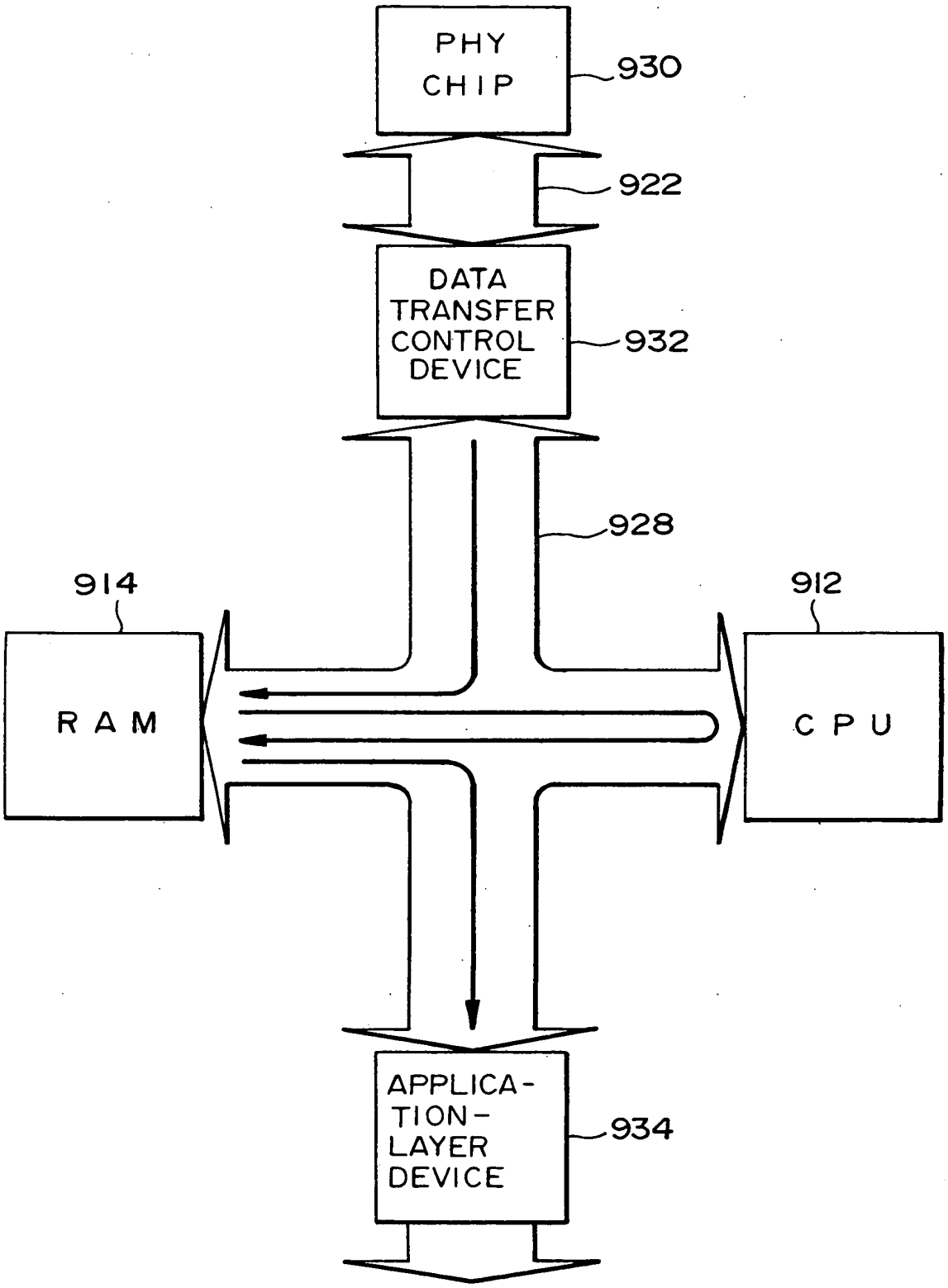
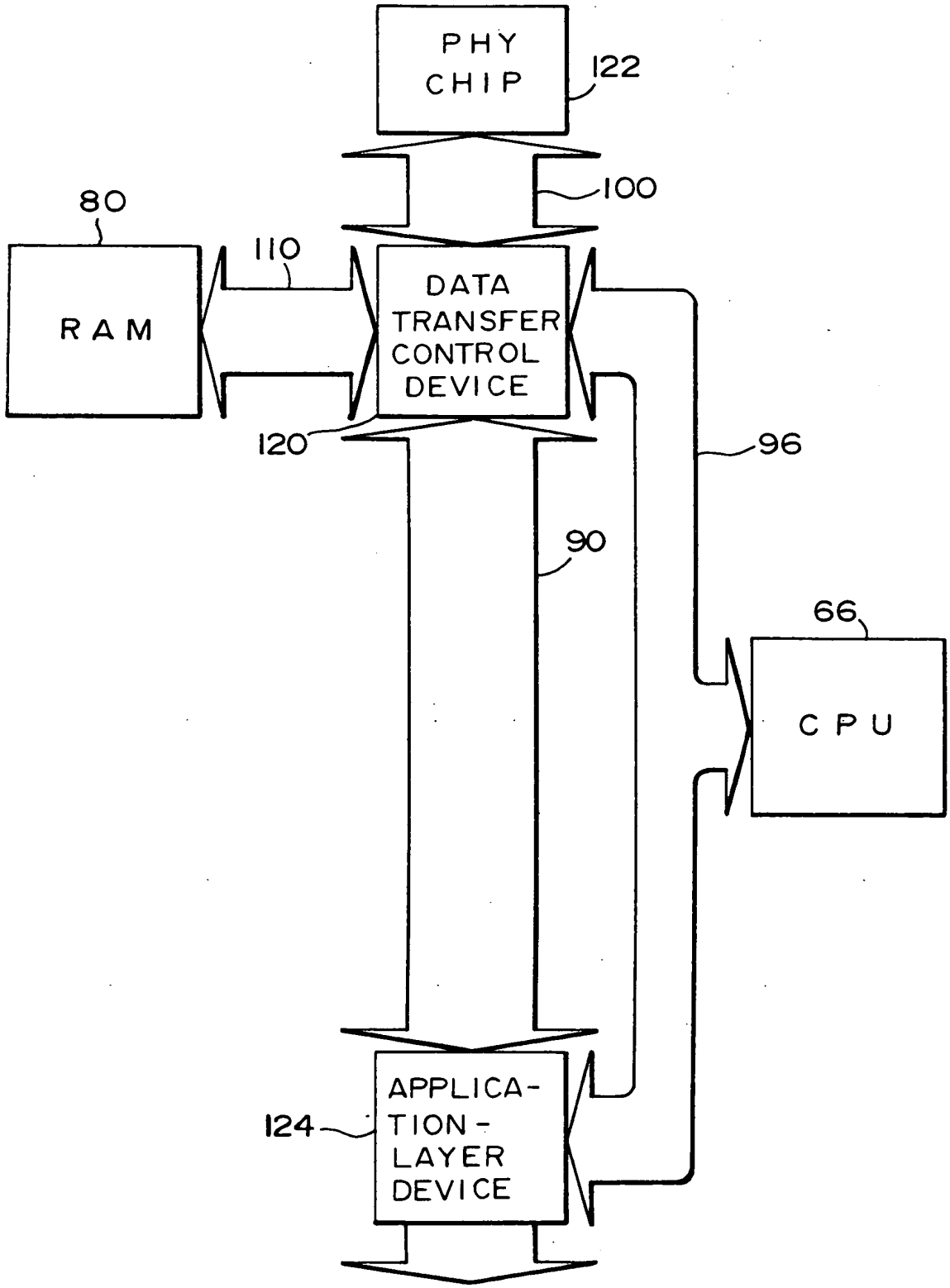

PHY CHIP
930
922
DATA TRANSFER CONTROL DEVICE
932
928
914
912
RAM
CPU
APPLICA-TION-LAYER DEVICE
934

FIG. 11


PHY CHIP
122
100
80
110
RAM
DATA TRANSFER CONTROL DEVICE
120
96
90
66
CPU
124
APPLICA-TION-LAYER DEVICE

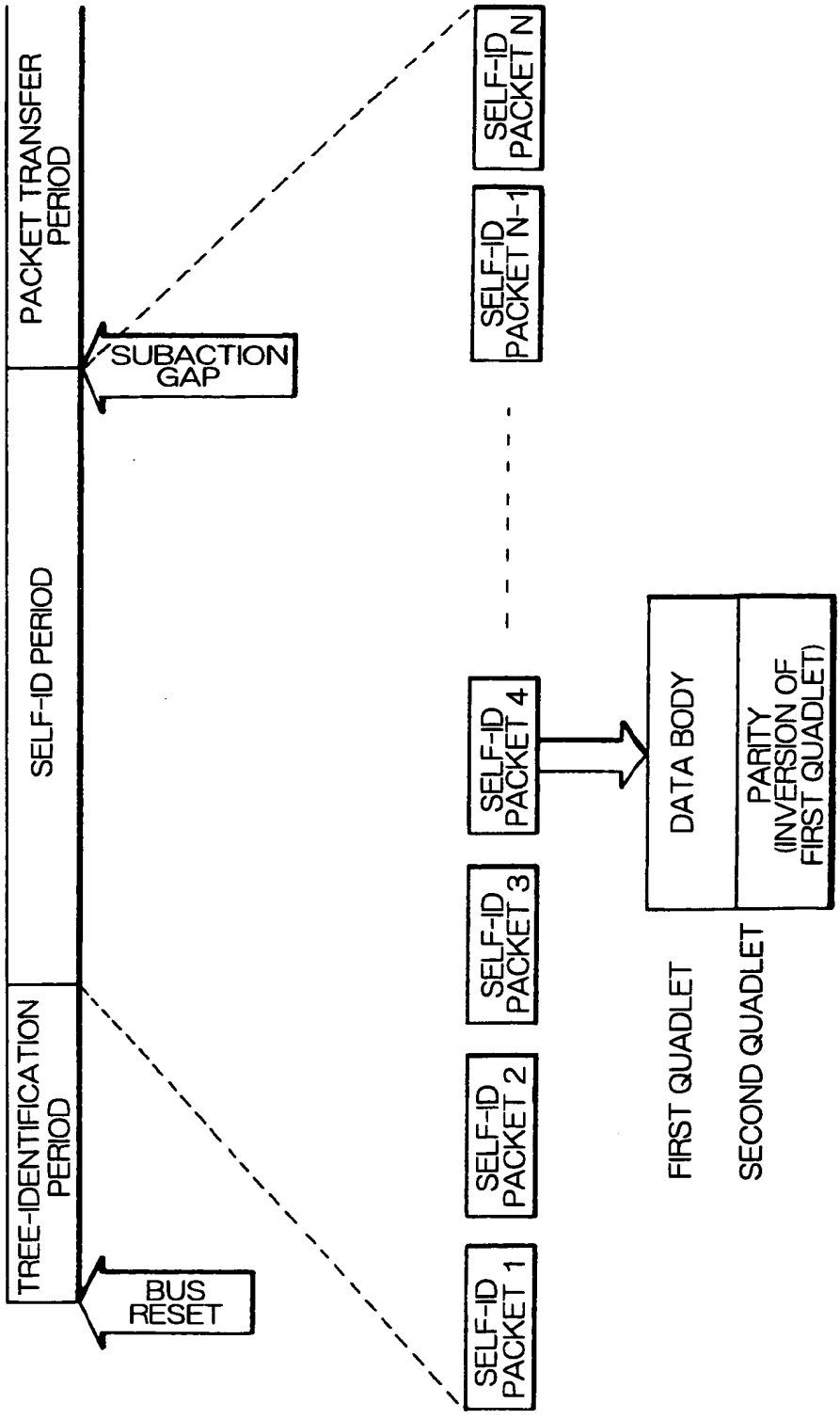

PACKET TRANSFER PERIOD
SUBACTION GAP
SELF-ID PERIOD
TREE-IDENTIFICATION PERIOD
BUS RESET
SELF-ID PACKET 1
SELF-ID PACKET 2
SELF-ID PACKET 3
SELF-ID PACKET 4
SELF-ID PACKET N-1
SELF-ID PACKET N
DATA BODY
PARITY (INVERSION OF FIRST QUADLET)
FIRST QUADLET
SECOND QUADLET

FIG. 12

FIG. 13A

COMPARATIVE EXAMPLE

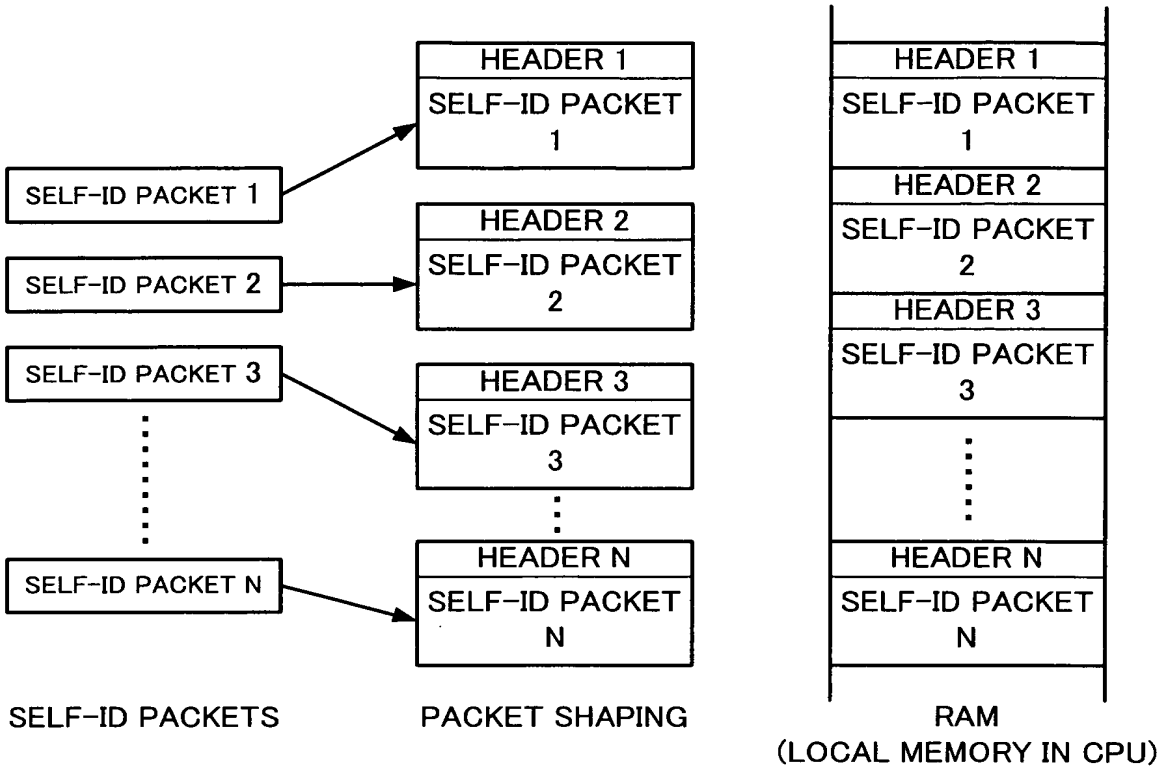


FIG. 13B

THIS EMBODIMENT OF THE PRESENT INVENTION

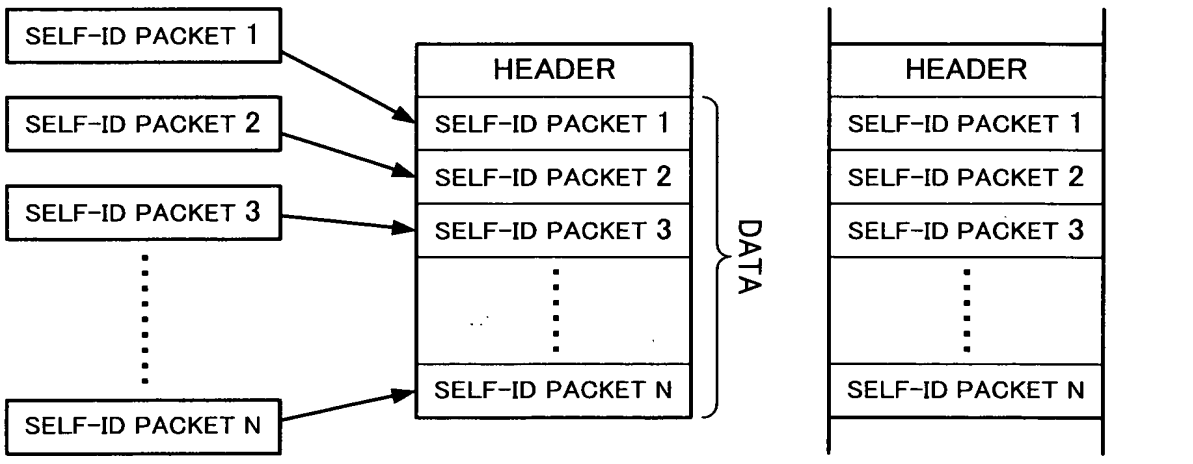


FIG. 14A

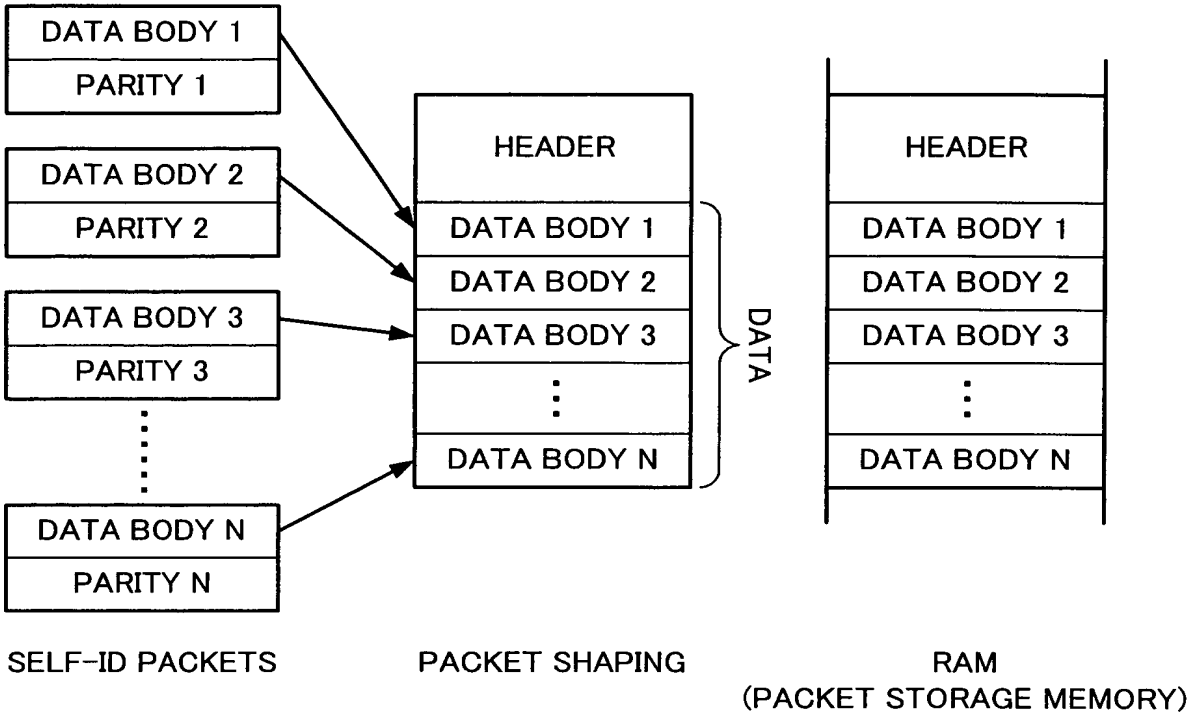


FIG. 14B

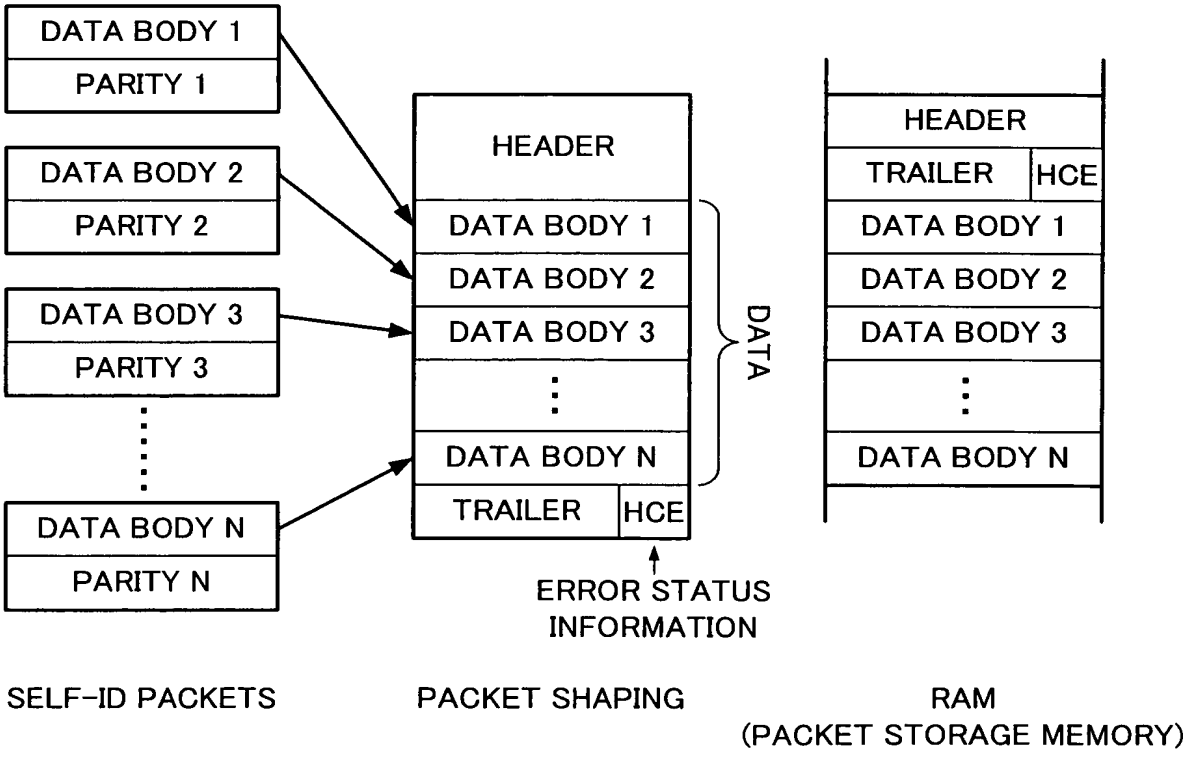


FIG. 15A

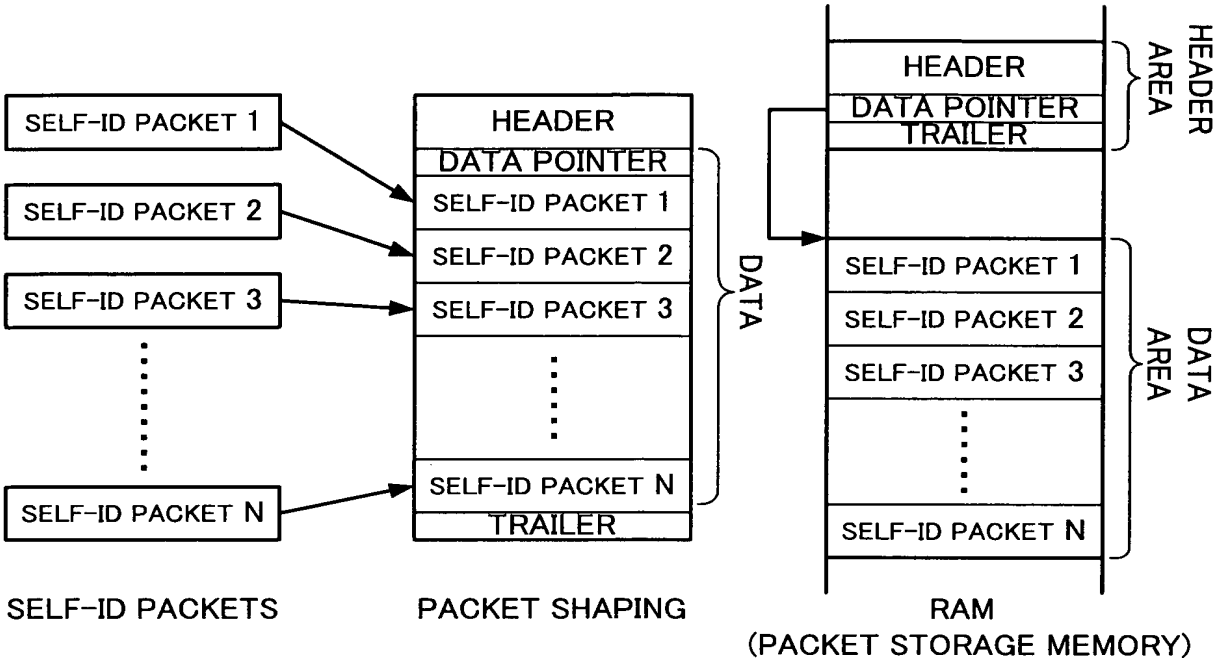


FIG. 15B

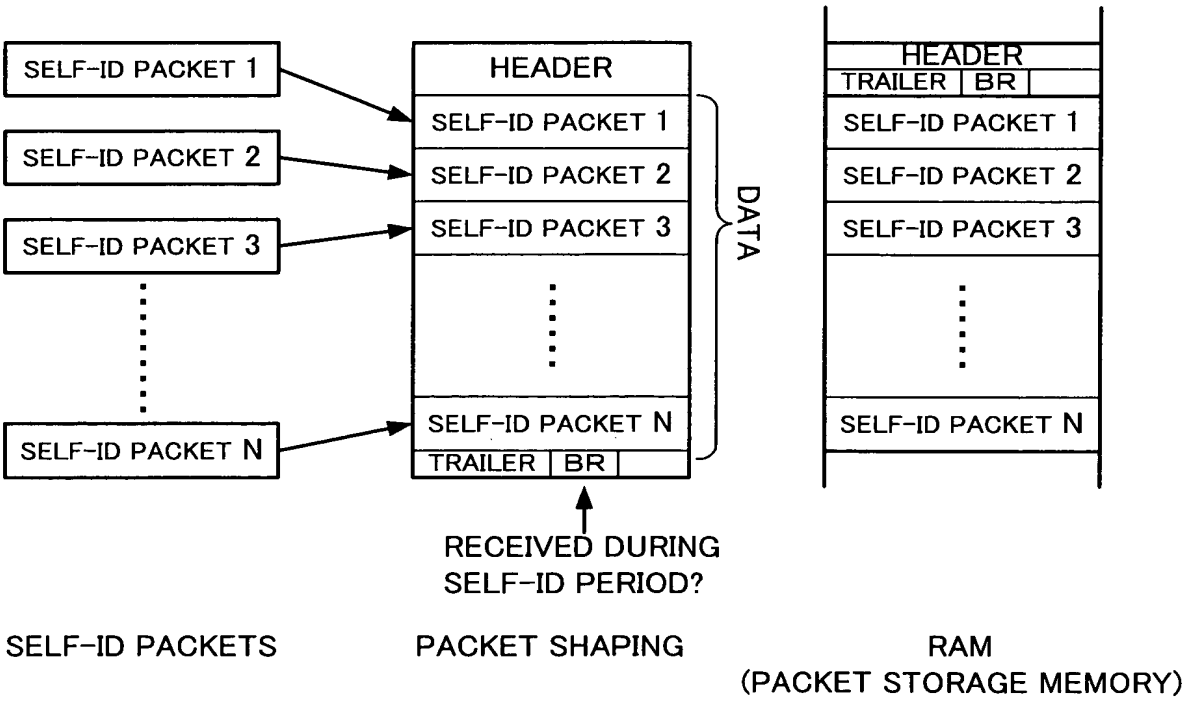
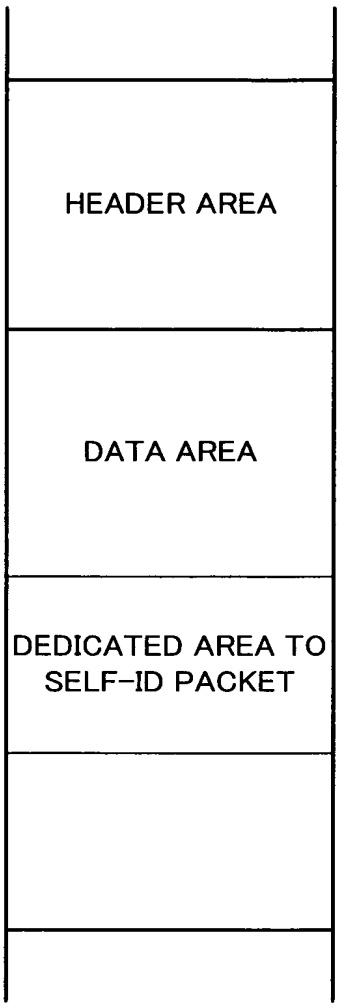


FIG. 16



RAM
(PACKET STORAGE MEMORY)

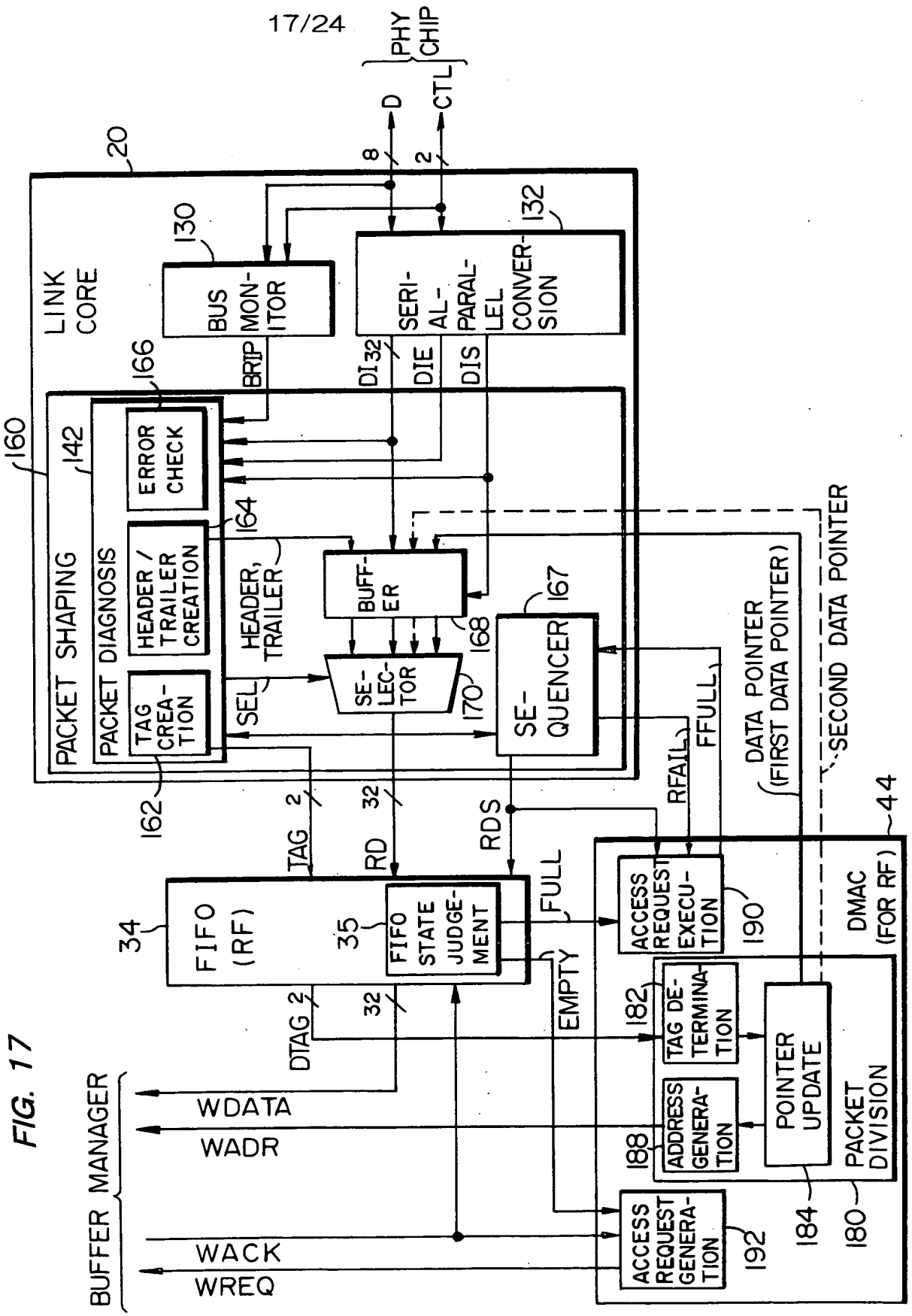

PHY CHIP
D
CTL
8
2
20
LINK CORE
130
BUS MONITOR
132
SERIAL-PARALLEL CONVERSION
BRIP
DI32
DIE
DIS
166
160
142
PACKET SHAPING
PACKET DIAGNOSIS
ERROR CHECK
HEADER / TRAILER CREATION
TAG CREATION
164
HEADER, TRAILER
BUFFER
168
167
SELECTOR
170
SEQUENCER
SEL
RFAIL
FFULL
DATA POINTER (FIRST DATA POINTER)
SECOND DATA POINTER
162
TAG 2
RD 32
RDS
44
34
FIFO (RF)
35
FIFO STATE JUDGEMENT
FULL
EMPTY
ACCESS REQUEST EXECUTION
190
DMAC (FOR RF)
DTAG 2
32
182
TAG DETERMINATION
POINTER UPDATE
PACKET DIVISION
188
ADDRESS GENERATION
184
180
ACCESS REQUEST GENERATION
192
BUFFER MANAGER
WDATA
WADR
WACK
WREQ

FIG. 17

FIG.18

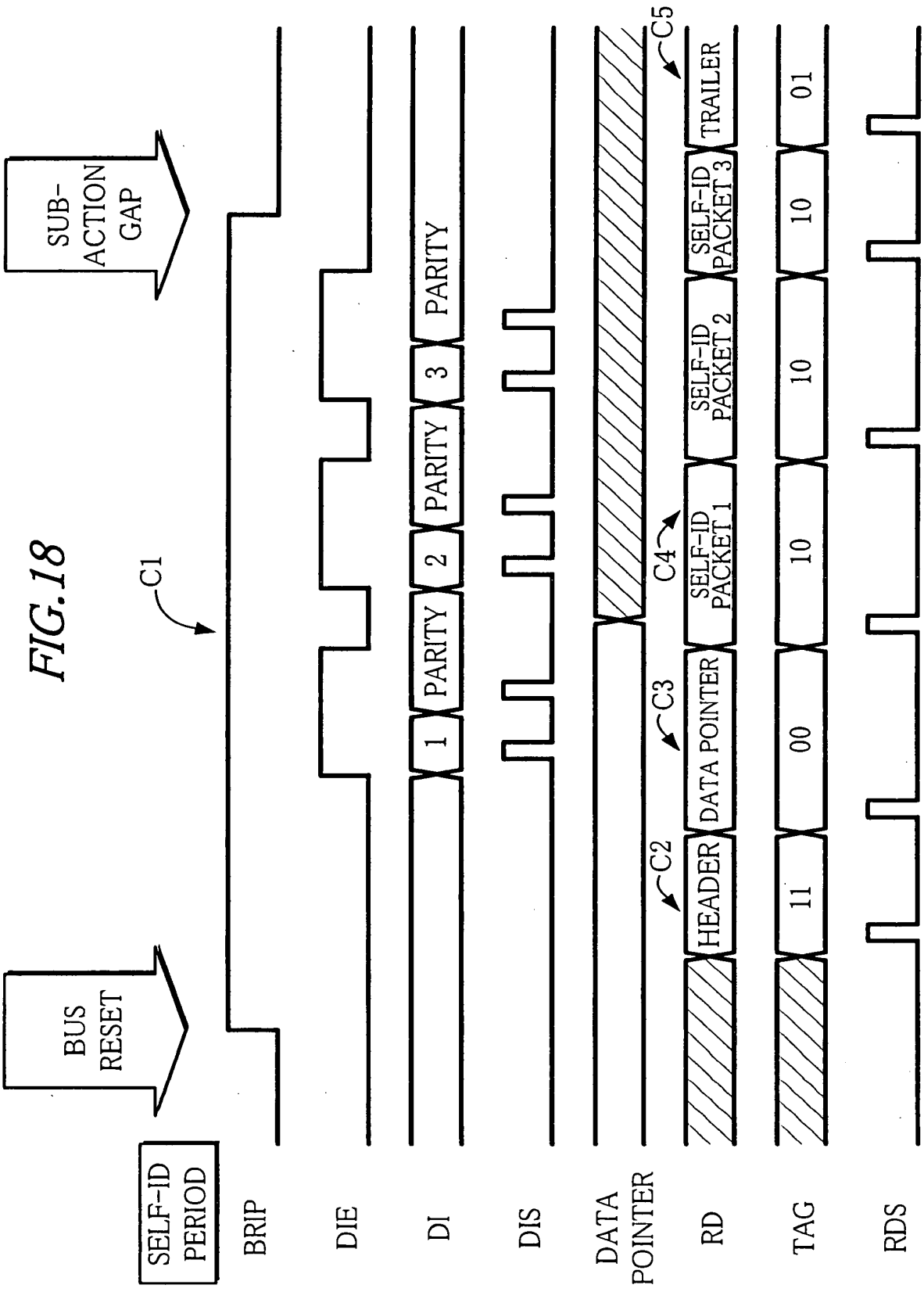

SELF-ID PERIOD
BUS RESET
SUB-ACTION GAP
C1
C2
C3
C4
C5
BRIP
DIE
DI
DIS
DATA POINTER
RD
TAG
RDS
1
PARITY
2
PARITY
3
PARITY
HEADER
DATA POINTER
SELF-ID PACKET 1
SELF-ID PACKET 2
SELF-ID PACKET 3
TRAILER
11
00
10
10
10
01

FIG. 19A

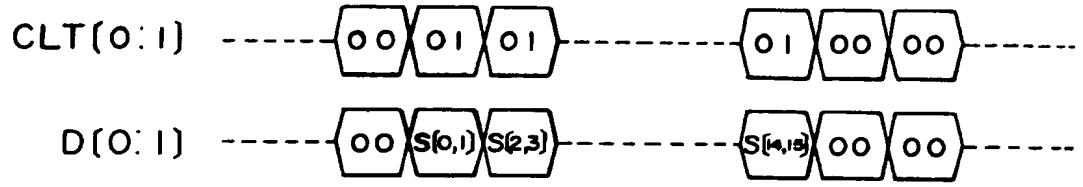


FIG. 19B

CTL WHILE PHY CHIP DRIVES

CTL	NAME
0 0	IDLE
0 1	STATUS
1 0	RECEIVE
1 1	GRANT

FIG. 19C

STATUS BITS

BIT	NAME
0	ARBITRATION RESET GAP
1	SUBACTION GAP
2	BUS RESET
3	PHY INTERRUPT
4 TO 7	ADDRESS
8 TO 15	DATA

FIG. 20A

RxAsynchronousBusResetPacket (tcode:0xE)

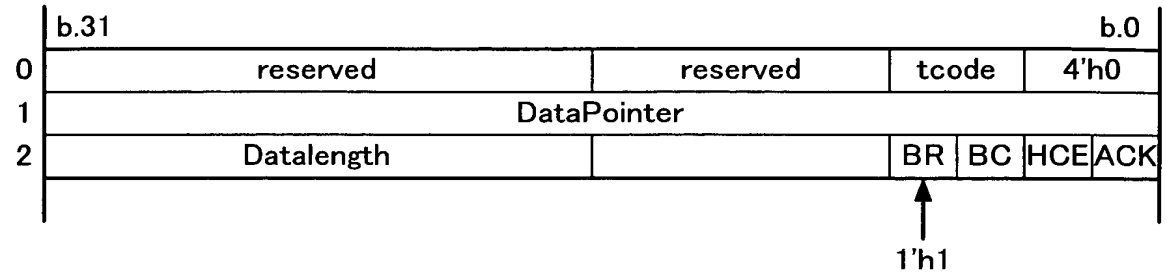


FIG. 20B

RxAsynchronousPhyPacket Nomal (tcode:0xE)

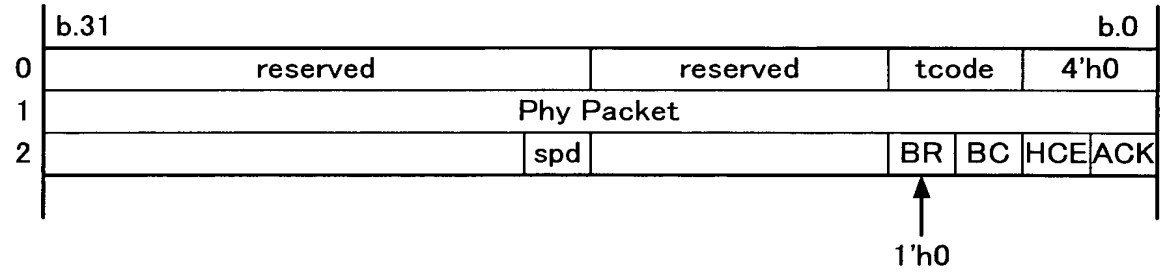


FIG. 21

TAG (DTAG)	MEANING
0 0	HEADER
0 1	TRAILER
1 0	DATA
1 1	START

FIG.22

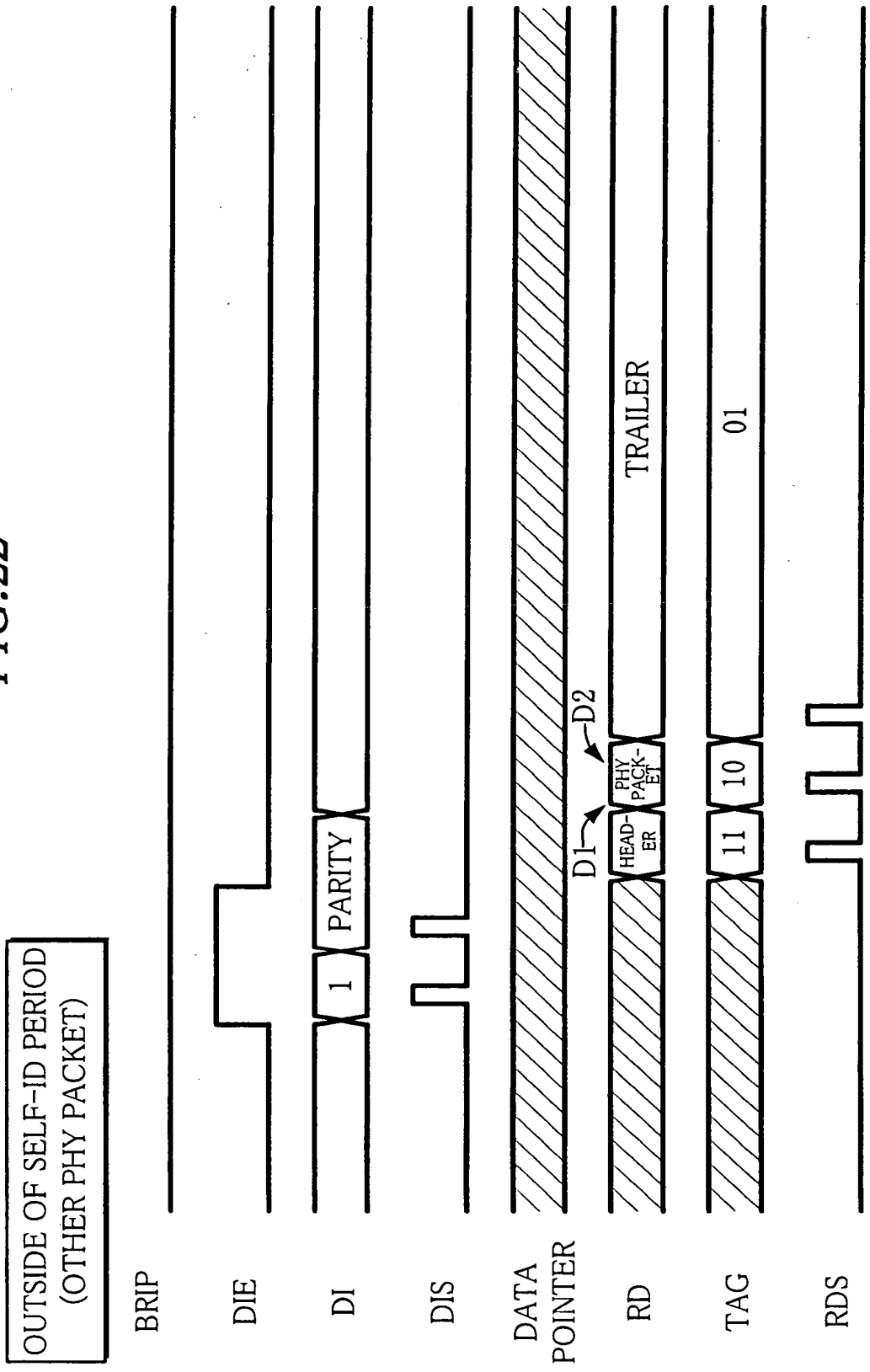

OUTSIDE OF SELF-ID PERIOD
(OTHER PHY PACKET)
BRIP
DIE
DI
1
PARITY
DIS
DATA
POINTER
D1
D2
HEAD-
ER
PHY
PACK-
ET
TRAILER
RD
TAG
11
10
01
RDS

FIG. 23A

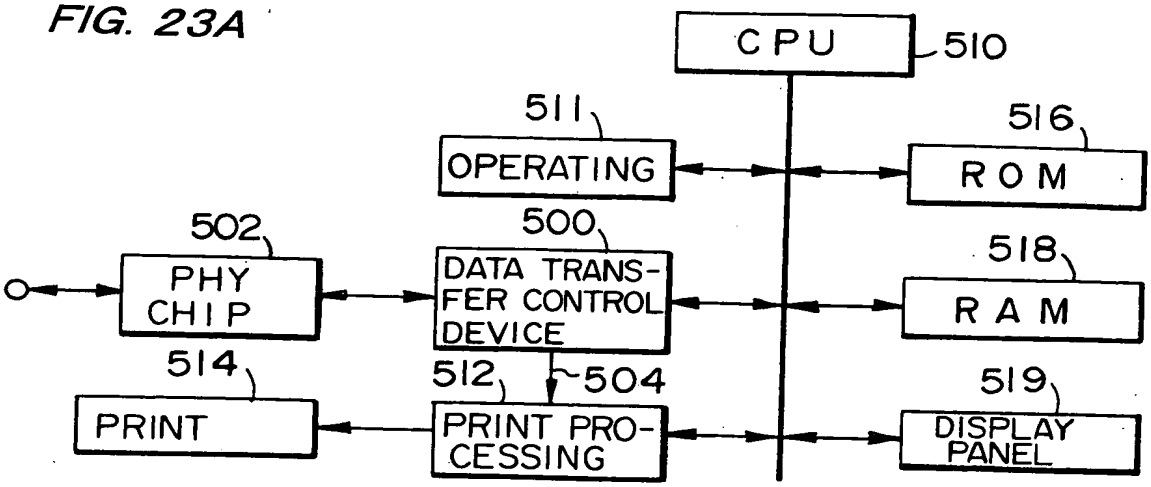


FIG. 23B

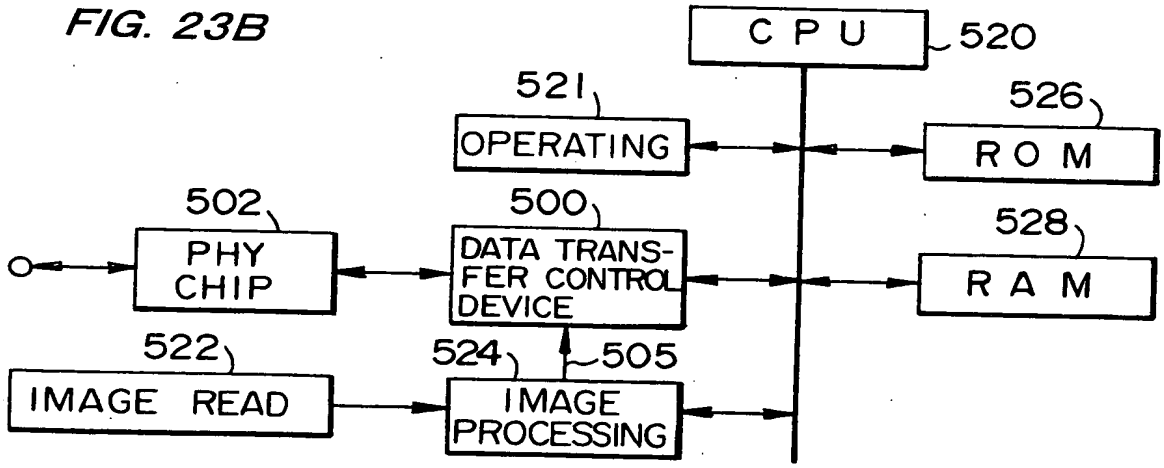


FIG. 23C

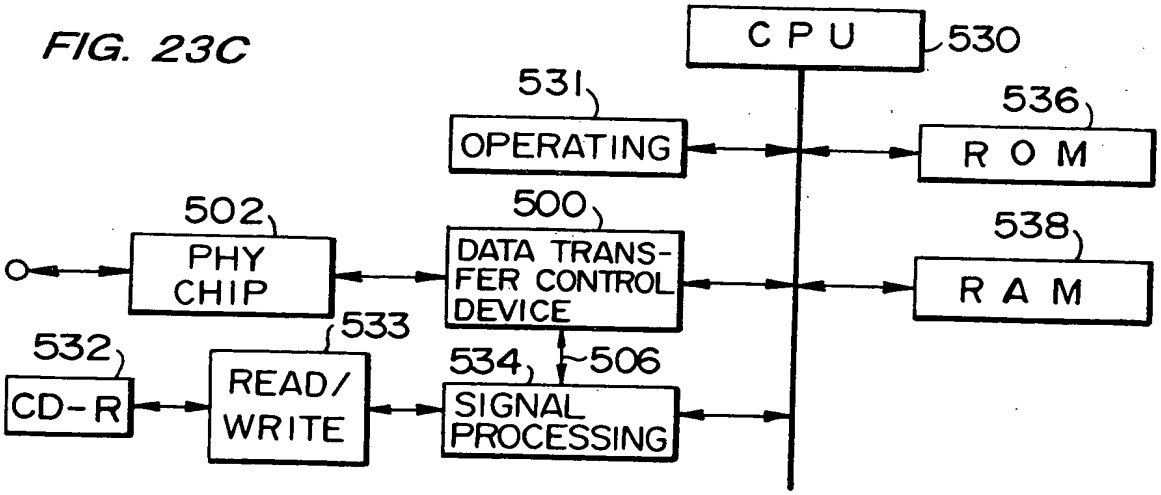


FIG. 24A

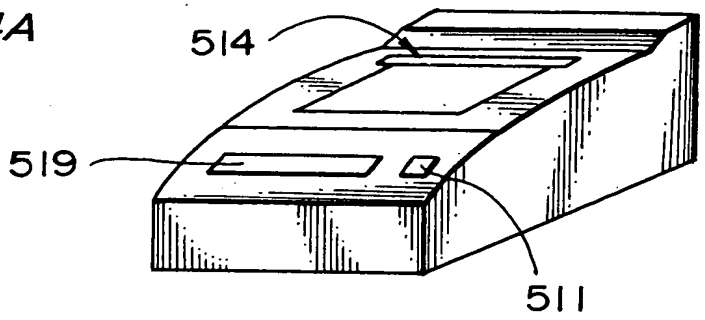


FIG. 24B

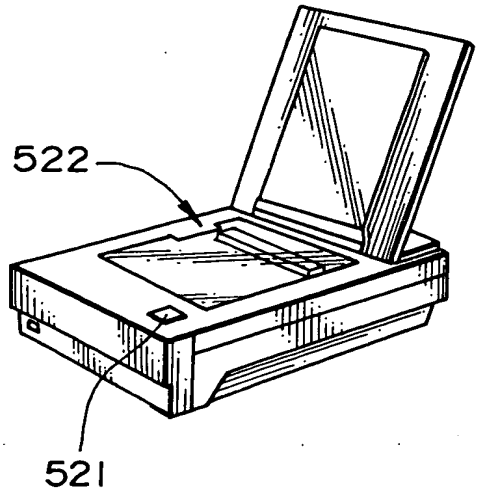
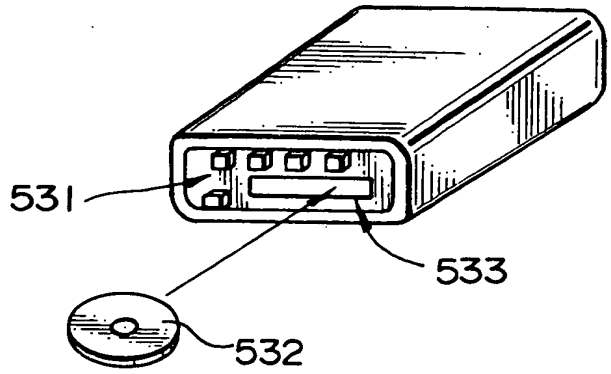



FIG. 24C